In the past a Verilog model for a SAP was created based on the basic understanding of MARIE Virtual Processor Learning Tool Employed in teaching computer organization and architecture classes.

With the need for students to learn Arm was viable tool for future development this module was created by Voltaire Dupo. It is hoped that students may find it more useful for systems development and add to it in the future making the architecture type no longer SAP centric only but also include the architecture types as inspired by the Acorn Research Machines Group.

Processor Block Diagram

A diagram of a computer circuit

Description automatically generated

Reference Tables for I/O Functions

addr: 5 bit input that can reference the 32 different memory locations

cpc: 2: PC will increment only once if CEENZ = 1 if its CEENZ = 0 then PC increments twice

1: PC will increment automatically every clk cycle.

0: no increment takes place

Reference Tables for I/O Functions

cmsrc: 0: muxout=R0;

1: muxout=R1;

2: muxout=R2;

3: muxout=R3;

4: muxout=R4;

5: muxout=R5;

6: muxout=R6;

8: muxout=CEE(ALU OUT;

csrc: 0: data\_in is the source of data to be stored

1: Literal is the source of data to be stored

2: MUXOUT is the source of data to be stored.

3: CEE or ALU Output is the source of data to be stored

Wr\_en: 1: allows write operations to memory

0: prevents any write operations to the memory

Reference Tables for I/O Functions

Calu: 01H: CEE = R1 + R2; // C=A+B

02H: CEE= R1 – R2; // C=A-B

03H: CEE = R1 \* R2; // C = A\*B

04H: CEE = ~R1; // NOT A

05H: CEE = R1 && R2; // AND

06H: CEE = R1 || R2; // OR

07H: CEE = R1 ^ R2; // XOR

08H: CEE = ~CEE; // C = NOT C

11H: CEE = R1 + Lit; // C=A+B

12H: CEE= R1 – Lit; // C=A-B

13H: CEE = R1 \* Lit; // C = A\*B

15H: CEE = R1 && Lit; // AND

16H: CEE = R1 || Lit; // OR

17H: CEE = R1 ^ Lit; // XOR

Code Guide

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Neumonic | CALU | CPC | WR\_EN | CMSRC | CSRC | Lit | Addr | Rst |
| MV R0,R0 | 0 | 1 | 1 | 0 | 2 | xx | 0 | 1 |
| MV R0,R1 | 0 | 1 | 1 | 1 | 2 | xx | 0 | 1 |
| MV R0,R2 | 0 | 1 | 1 | 2 | 2 | xx | 0 | 1 |
| MV R0,R3 | 0 | 1 | 1 | 3 | 2 | xx | 0 | 1 |
| MV R0,R4 | 0 | 1 | 1 | 4 | 2 | xx | 0 | 1 |
| MV R0,R5 | 0 | 1 | 1 | 5 | 2 | xx | 0 | 1 |
| MV R0,R6 | 0 | 1 | 1 | 6 | 2 | xx | 0 | 1 |
| MV R1,CEE | 0 | 1 | 1 | 7 | 2 | xx | 0 | 1 |
| MV R1,R0 | 0 | 1 | 1 | 0 | 2 | xx | 1 | 1 |
| MV R1,R1 | 0 | 1 | 1 | 1 | 2 | xx | 1 | 1 |
| MV R1,R2 | 0 | 1 | 1 | 2 | 2 | xx | 1 | 1 |
| MV R1,R3 | 0 | 1 | 1 | 3 | 2 | xx | 1 | 1 |
| MV R1,R4 | 0 | 1 | 1 | 4 | 2 | xx | 1 | 1 |
| MV R1,R5 | 0 | 1 | 1 | 5 | 2 | xx | 1 | 1 |
| MV R1,R6 | 0 | 1 | 1 | 6 | 2 | xx | 1 | 1 |
| MV R1,CEE | 0 | 1 | 1 | 7 | 2 | xx | 1 | 1 |
| MV R2,R0 | 0 | 1 | 1 | 0 | 2 | xx | 2 | 1 |
| MV R2,R1 | 0 | 1 | 1 | 1 | 2 | xx | 2 | 1 |
| MV R2,R2 | 0 | 1 | 1 | 2 | 2 | xx | 2 | 1 |
| MV R2,R3 | 0 | 1 | 1 | 3 | 2 | xx | 2 | 1 |
| MV R2,R4 | 0 | 1 | 1 | 4 | 2 | xx | 2 | 1 |
| MV R2,R5 | 0 | 1 | 1 | 5 | 2 | xx | 2 | 1 |
| MV R2,R6 | 0 | 1 | 1 | 6 | 2 | xx | 2 | 1 |
| MV R  2,CEE | 0 | 1 | 1 | 7 | 2 | xx | 2 | 1 |
| MV R3,R0 | 0 | 1 | 1 | 0 | 2 | xx | 3 | 1 |
| MV R3,R1 | 0 | 1 | 1 | 1 | 2 | xx | 3 | 1 |
| MV R3,R2 | 0 | 1 | 1 | 2 | 2 | xx | 3 | 1 |
| MV R3,R3 | 0 | 1 | 1 | 3 | 2 | xx | 3 | 1 |
| MV R3,R4 | 0 | 1 | 1 | 4 | 2 | xx | 3 | 1 |
| MV R3,R5 | 0 | 1 | 1 | 5 | 2 | xx | 3 | 1 |
| MV R3,R6 | 0 | 1 | 1 | 6 | 2 | xx | 3 | 1 |
| MV R3,CEE | 0 | 1 | 1 | 7 | 2 | xx | 3 | 1 |
| MV R4,R0 | 0 | 1 | 1 | 0 | 2 | xx | 4 | 1 |
| MV R4,R1 | 0 | 1 | 1 | 1 | 2 | xx | 4 | 1 |
| MV R4,R2 | 0 | 1 | 1 | 2 | 2 | xx | 4 | 1 |
| MV R4,R3 | 0 | 1 | 1 | 3 | 2 | xx | 4 | 1 |
| MV R4,R4 | 0 | 1 | 1 | 4 | 2 | xx | 4 | 1 |
| MV R4,R5 | 0 | 1 | 1 | 5 | 2 | xx | 4 | 1 |
| MV R4,R6 | 0 | 1 | 1 | 6 | 2 | xx | 4 | 1 |
| MV R4,CEE | 0 | 1 | 1 | 7 | 2 | xx | 4 | 1 |
| MV R5,R0 | 0 | 1 | 1 | 0 | 2 | xx | 5 | 1 |
| MV R5,R1 | 0 | 1 | 1 | 1 | 2 | xx | 5 | 1 |

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Neumonic | CALU | CPC | WR\_EN | CMSRC | CSRC | Lit | Addr | Rst |
| MV R5,R2 | 0 | 1 | 1 | 2 | 2 | xx | 5 | 1 |
| MV R5,R3 | 0 | 1 | 1 | 3 | 2 | xx | 5 | 1 |
| MV R5,R4 | 0 | 1 | 1 | 4 | 2 | xx | 5 | 1 |
| MV R5,R5 | 0 | 1 | 1 | 5 | 2 | xx | 5 | 1 |
| MV R5,R6 | 0 | 1 | 1 | 6 | 2 | xx | 5 | 1 |
| MV R5,CEE | 0 | 1 | 1 | 7 | 2 | xx | 5 | 1 |
| MV R6,R0 | 0 | 1 | 1 | 0 | 2 | xx | 6 | 1 |
| MV R6,R1 | 0 | 1 | 1 | 1 | 2 | xx | 6 | 1 |
| MV R6,R2 | 0 | 1 | 1 | 2 | 2 | xx | 6 | 1 |
| MV R6,R3 | 0 | 1 | 1 | 3 | 2 | xx | 6 | 1 |
| MV R6,R4 | 0 | 1 | 1 | 4 | 2 | xx | 6 | 1 |
| MV R6,R5 | 0 | 1 | 1 | 5 | 2 | xx | 6 | 1 |
| MV R6,R6 | 0 | 1 | 1 | 6 | 2 | xx | 6 | 1 |
| MV R6,CEE | 0 | 1 | 1 | 7 | 2 | xx | 6 | 1 |
| LD R0,IN | 0 | 1 | 1 | 0 | 0 | xx | 0 | 1 |
| LD R1,IN | 0 | 1 | 1 | 0 | 0 | xx | 1 | 1 |
| LD R2,IN | 0 | 1 | 1 | 0 | 0 | xx | 2 | 1 |
| LD R3,IN | 0 | 1 | 1 | 0 | 0 | xx | 3 | 1 |
| LD R4,IN | 0 | 1 | 1 | 0 | 0 | xx | 4 | 1 |
| LD R5,IN | 0 | 1 | 1 | 0 | 0 | xx | 5 | 1 |
| LD R6,IN | 0 | 1 | 1 | 0 | 0 | xx | 6 | 1 |
| LD R0,Lit | 0 | 1 | 1 | 0 | 1 | Lit | 0 | 1 |
| LD R1,Lit | 0 | 1 | 1 | 0 | 1 | Lit | 0 | 1 |
| LD R2,Lit | 0 | 1 | 1 | 0 | 1 | Lit | 0 | 1 |
| LD R3,Lit | 0 | 1 | 1 | 0 | 1 | Lit | 3 | 1 |
| LD R4,Lit | 0 | 1 | 1 | 0 | 1 | Lit | 4 | 1 |
| LD R5,Lit | 0 | 1 | 1 | 0 | 1 | Lit | 5 | 1 |
| LD R6,Lit | 0 | 1 | 1 | 0 | 1 | Lit | 6 | 1 |
| AD R0,R1,R2 | 1 | 1 | 1 | 0 | 3 | xx | 0 | 1 |
| AD R1,R1,R2 | 1 | 1 | 1 | 0 | 3 | xx | 1 | 1 |
| AD R2,R1,R2 | 1 | 1 | 1 | 0 | 3 | xx | 2 | 1 |
| AD R3,R1,R2 | 1 | 1 | 1 | 0 | 3 | xx | 3 | 1 |
| AD R4,R1,R2 | 1 | 1 | 1 | 0 | 3 | xx | 4 | 1 |
| AD R5,R1,R2 | 1 | 1 | 1 | 0 | 3 | xx | 5 | 1 |
| AD R6,R1,R2 | 1 | 1 | 1 | 0 | 3 | xx | 6 | 1 |
| SB R0,R1,R2 | 2 | 1 | 1 | 0 | 3 | xx | 0 | 1 |
| SB R1,R1,R2 | 2 | 1 | 1 | 0 | 3 | xx | 1 | 1 |
| SB R2,R1,R2 | 2 | 1 | 1 | 0 | 3 | xx | 2 | 1 |
| SB R3,R1,R2 | 2 | 1 | 1 | 0 | 3 | xx | 3 | 1 |
| SB R4,R1,R2 | 2 | 1 | 1 | 0 | 3 | xx | 4 | 1 |
| SB R5,R1,R2 | 2 | 1 | 1 | 0 | 3 | xx | 5 | 1 |
| SB R6,R1,R2 | 2 | 1 | 1 | 0 | 3 | xx | 6 | 1 |
| ML R0,R1,R2 | 3 | 1 | 1 | 0 | 3 | xx | 0 | 1 |
| ML R1,R1,R2 | 3 | 1 | 1 | 0 | 3 | xx | 1 | 1 |
| ML R2,R1,R2 | 3 | 1 | 1 | 0 | 3 | xx | 2 | 1 |
| ML R3,R1,R2 | 3 | 1 | 1 | 0 | 3 | xx | 3 | 1 |
| ML R4,R1,R2 | 3 | 1 | 1 | 0 | 3 | xx | 4 | 1 |
| ML R5,R1,R2 | 3 | 1 | 1 | 0 | 3 | xx | 5 | 1 |
| ML R6,R1,R2 | 3 | 1 | 1 | 0 | 3 | xx | 6 | 1 |
| & R0,R1,R2 | 5 | 1 | 1 | 0 | 3 | xx | 0 | 1 |
| & R1,R1,R2 | 5 | 1 | 1 | 0 | 3 | xx | 1 | 1 |
| & R2,R1,R2 | 5 | 1 | 1 | 0 | 3 | xx | 2 | 1 |
| & R3,R1,R2 | 5 | 1 | 1 | 0 | 3 | xx | 3 | 1 |
| & R4,R1,R2 | 5 | 1 | 1 | 0 | 3 | xx | 4 | 1 |
| & R5,R1,R2 | 5 | 1 | 1 | 0 | 3 | xx | 5 | 1 |
| & R6,R1,R2 | 5 | 1 | 1 | 0 | 3 | xx | 6 | 1 |

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Neumonic | CALU | CPC | WR\_EN | CMSRC | CSRC | Lit | Addr | Rst |
| | R0,R1,R2 | 6 | 1 | 1 | 0 | 3 | xx | 0 | 1 |
| | R1,R1,R2 | 6 | 1 | 1 | 0 | 3 | xx | 1 | 1 |
| | R2,R1,R2 | 6 | 1 | 1 | 0 | 3 | xx | 2 | 1 |
| | R3,R1,R2 | 6 | 1 | 1 | 0 | 3 | xx | 3 | 1 |
| | R4,R1,R2 | 6 | 1 | 1 | 0 | 3 | xx | 4 | 1 |
| | R5,R1,R2 | 6 | 1 | 1 | 0 | 3 | xx | 5 | 1 |
| | R6,R1,R2 | 6 | 1 | 1 | 0 | 3 | xx | 6 | 1 |
| ^ R0,R1,R2 | 7 | 1 | 1 | 0 | 3 | xx | 0 | 1 |
| ^ R1,R1,R2 | 7 | 1 | 1 | 0 | 3 | xx | 1 | 1 |
| ^ R2,R1,R2 | 7 | 1 | 1 | 0 | 3 | xx | 2 | 1 |
| ^ R3,R1,R2 | 7 | 1 | 1 | 0 | 3 | xx | 3 | 1 |
| ^ R4,R1,R2 | 7 | 1 | 1 | 0 | 3 | xx | 4 | 1 |
| ^ R5,R1,R2 | 7 | 1 | 1 | 0 | 3 | xx | 5 | 1 |
| ^ R6,R1,R2 | 7 | 1 | 1 | 0 | 3 | xx | 6 | 1 |
| ~ R0,R1 | 4 | 1 | 1 | 0 | 3 | xx | 0 | 1 |
| ~ R1,R1 | 4 | 1 | 1 | 0 | 3 | xx | 1 | 1 |
| ~ R2,R1 | 4 | 1 | 1 | 0 | 3 | xx | 2 | 1 |
| ~ R3,R1 | 4 | 1 | 1 | 0 | 3 | xx | 3 | 1 |
| ~ R4,R1 | 4 | 1 | 1 | 0 | 3 | xx | 4 | 1 |
| ~ R5,R1 | 4 | 1 | 1 | 0 | 3 | xx | 5 | 1 |
| ~ R6,R1 | 4 | 1 | 1 | 0 | 3 | xx | 6 | 1 |
| ~ R0,CEE | 8 | 1 | 1 | 0 | 3 | xx | 0 | 1 |
| ~ R1,CEE | 8 | 1 | 1 | 0 | 3 | xx | 1 | 1 |
| ~ R2,CEE | 8 | 1 | 1 | 0 | 3 | xx | 2 | 1 |
| ~ R3,CEE | 8 | 1 | 1 | 0 | 3 | xx | 3 | 1 |
| ~ R4,CEE | 8 | 1 | 1 | 0 | 3 | xx | 4 | 1 |
| ~ R5,CEE | 8 | 1 | 1 | 0 | 3 | xx | 5 | 1 |
| ~ R6,CEE | 8 | 1 | 1 | 0 | 3 | xx | 6 | 1 |
| JMP Addr | 0 | 0 | 1 | 0 | 1 | Addr | -------- | 1 |

Decision Making

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Neumonic | CALU | CPC | WR\_EN | CMSRC | CSRC | Lit | Addr | Rst |
| CMP R1,Lit | 0 | 2 | 1 | 0 | 0 | xx | 31d | 1 |
| Yes Same | 6 | X | 1 | 0 | 0 | xx | 31d | 1 |
| Not the Same | 6 | X | 1 | 0 | 0 | xx | 31d | 1 |

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Neumonic | CALU | CPC | WR\_EN | CMSRC | CSRC | Lit | Addr | Rst |
| AD R0,R1,Lit | 11 | 1 | 1 | 0 | 3 | Lit | 0 | 1 |
| AD R1,R1,Lit | 11 | 1 | 1 | 0 | 3 | Lit | 1 | 1 |
| AD R2,R1,Lit | 11 | 1 | 1 | 0 | 3 | Lit | 2 | 1 |
| AD R3,R1,Lit | 11 | 1 | 1 | 0 | 3 | Lit | 3 | 1 |
| AD R4,R1,Lit | 11 | 1 | 1 | 0 | 3 | Lit | 4 | 1 |
| AD R5,R1,Lit | 11 | 1 | 1 | 0 | 3 | Lit | 5 | 1 |
| AD R6,R1,Lit | 11 | 1 | 1 | 0 | 3 | Lit | 6 | 1 |
| SB R0,R1,Lit | 12 | 1 | 1 | 0 | 3 | Lit | 0 | 1 |
| SB R1,R1,Lit | 12 | 1 | 1 | 0 | 3 | Lit | 1 | 1 |
| SB R2,R1,Lit | 12 | 1 | 1 | 0 | 3 | Lit | 2 | 1 |
| SB R3,R1,Lit | 12 | 1 | 1 | 0 | 3 | Lit | 3 | 1 |
| SB R4,R1,Lit | 12 | 1 | 1 | 0 | 3 | Lit | 4 | 1 |
| SB R5,R1,Lit | 12 | 1 | 1 | 0 | 3 | Lit | 5 | 1 |
| SB R6,R1,Lit | 12 | 1 | 1 | 0 | 3 | Lit | 6 | 1 |
| ML R0,R1,Lit | 13 | 1 | 1 | 0 | 3 | Lit | 0 | 1 |
| ML R1,R1,Lit | 13 | 1 | 1 | 0 | 3 | Lit | 1 | 1 |
| ML R2,R1,Lit | 13 | 1 | 1 | 0 | 3 | Lit | 2 | 1 |
| ML R3,R1,Lit | 13 | 1 | 1 | 0 | 3 | Lit | 3 | 1 |
| ML R4,R1,Lit | 13 | 1 | 1 | 0 | 3 | Lit | 4 | 1 |
| ML R5,R1,Lit | 13 | 1 | 1 | 0 | 3 | Lit | 5 | 1 |
| ML R6,R1,Lit | 13 | 1 | 1 | 0 | 3 | Lit | 6 | 1 |
| & R0,R1,Lit | 15 | 1 | 1 | 0 | 3 | Lit | 0 | 1 |
| & R1,R1,Lit | 15 | 1 | 1 | 0 | 3 | Lit | 1 | 1 |
| & R2,R1,Lit | 15 | 1 | 1 | 0 | 3 | Lit | 2 | 1 |
| & R3,R1,Lit | 15 | 1 | 1 | 0 | 3 | Lit | 3 | 1 |
| & R4,R1,Lit | 15 | 1 | 1 | 0 | 3 | Lit | 4 | 1 |
| & R5,R1,Lit | 15 | 1 | 1 | 0 | 3 | Lit | 5 | 1 |
| & R6,R1,Lit | 15 | 1 | 1 | 0 | 3 | Lit | 6 | 1 |
| | R0,R1,Lit | 16 | 1 | 1 | 0 | 3 | Lit | 0 | 1 |
| | R1,R1,Lit | 16 | 1 | 1 | 0 | 3 | Lit | 1 | 1 |
| | R2,R1,Lit | 16 | 1 | 1 | 0 | 3 | Lit | 2 | 1 |
| | R3,R1,Lit | 16 | 1 | 1 | 0 | 3 | Lit | 3 | 1 |
| | R4,R1,Lit | 16 | 1 | 1 | 0 | 3 | Lit | 4 | 1 |
| | R5,R1,Lit | 16 | 1 | 1 | 0 | 3 | Lit | 5 | 1 |
| | R6,R1,Lit | 16 | 1 | 1 | 0 | 3 | Lit | 6 | 1 |
| ^ R0,R1,Lit | 17 | 1 | 1 | 0 | 3 | Lit | 0 | 1 |
| ^ R1,R1,Lit | 17 | 1 | 1 | 0 | 3 | Lit | 1 | 1 |
| ^ R2,R1,Lit | 17 | 1 | 1 | 0 | 3 | Lit | 2 | 1 |
| ^ R3,R1,Lit | 17 | 1 | 1 | 0 | 3 | Lit | 3 | 1 |
| ^ R4,R1,Lit | 17 | 1 | 1 | 0 | 3 | Lit | 4 | 1 |
| ^ R5,R1,Lit | 17 | 1 | 1 | 0 | 3 | Lit | 5 | 1 |
| ^ R6,R1,Lit | 17 | 1 | 1 | 0 | 3 | Lit | 6 | 1 |